

PATENT
PF980092**CUSTOMER NO.: 24498****Serial No. 09/869,397**

Reply to Final Office Action dated: 2/01/06

Response dated: 6/08/06

REMARKS

In the Office Action, the Examiner noted that claims 1-8 are pending in the application and that claims 1-8 stand rejected. By this response, all claims continue unamended.

In view of the following discussion, the Applicant respectfully submits that none of the claims are anticipated under the provisions of 35 U.S.C. § 102 or rendered obvious under the provisions of 35 U.S.C. § 103. Thus the Applicant believes that all of these claims and the application are now in allowable form.

Rejections**A. 35 U.S.C. § 102**

The Examiner rejected claims 1-4, 6 and 7 under 35 U.S.C. § 102(e) as being anticipated by Thomason (U.S. Patent No. 6,018,612). The rejection is respectfully traversed.

Regarding claim 1, the Examiner alleges that Thomason discloses a process for recording a digital video and audio data stream wherein recording being carried out on a medium organized in the form of logic blocks in series and comprising a recording and reading head including all of the aspects of the Applicant's invention. The Applicant respectfully disagrees.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)). (emphasis added). The Applicant respectfully submits that Thomason fails to teach each and every element of at least the Applicant's claim 1, which specifically recites:

"A process for recording a digital video and audio data stream wherein recording being carried out on a medium organized in the form of logic blocks in series and comprising a recording and reading head, said process comprises the steps of:

recording data in one block out of two starting from a first block, following the triggering of the reading of the data, alternately reading a previously recorded block and continuing the recording in the block following the block read.

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The Applicant's claim 1 finds support throughout the specification. More specifically, Claim 1 is directed to a process for recording a digital video and audio data stream wherein recording being carried out on a medium (hard disk 201 on page 5, line 23) organized in the form of logic blocks in series and comprising a recording and reading head, the process including the steps of recording data in one block out of two starting from a first block (see figure 9a, page 18 lines 10-13) and following the triggering of the reading of the data, alternately reading a previously recorded block and continuing the recording in the block following the block read (see page 18 lines 14-21).

In contrast to the invention of the Applicant, at least as claimed by the Applicant's independent claim 1, Thomason describes a process for recording a digital video and audio data stream wherein recording is carried out on a medium (hard disk 36), organized in the form of logic blocks in series and comprising a recording and reading head (column 4 line 36), the process comprising the steps of storing first in a buffer memory (35) the data before transferring them to the main memory (36) and also, when reading data on the main memory (36), data is initially sent to the buffer memory (35). The Invention proposes a useful arrangement of the buffer memory in order to make the data transfers with the main memory using an efficient manner. However, the arrangement is dedicated to the management of the buffer memories and not to the arrangement of the main memory.

More specifically, In Thomason, and specifically referring to Figure 2, Thomason describes a main memory, which can be in the form of a band disk arrangement (see column 3 line 57) and can be a hard-disk (see column 3 line 9). This main memory is interfaced to the management of this memory with a buffer memory comprising an input buffer 35a, an output buffer 35b and a free space between these two buffers. A micro-processor initiates the data transfer from the buffer 4 to the buffer memory 35. Input data in the buffer memory 35 is transferred to the main memory 36 as soon as it is convenient under the supervision of the microprocessor 34....(see column 3 lines 60-67)...the stored data in main memory 36 is in due course transferred to the buffer memory 35 under supervision of the

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microprocessor 34... (see column 4 lines 1-3). Thomason teaches the management of the data in the buffer memory and not the management of the data in the main memory. That is, in Thomason, the buffer is divided in two parts and the blocks are read in one part and written in the other part. However, it is not the main memory which is written one block out of two as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. The Examiner specifically alleges that P1 and P2 are blocks but the Applicant respectfully submits that in Thomason, P1 and P2 are blocks of the buffer memory and not blocks of the main memory. In Thomason, the main memory is written in a conventional way, or at least it is not the object of Thomason as nothing is said in Thomason about the main memory.

The buffer memory of Thomason represents one embodiment to avoid having a delay induced by the movement of the head, the data being firstly stored in the buffer memory, so the buffer memory acts as a cache memory. However, it is not the same solution which is taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. In order to avoid having such an additional buffer (35), claim 1 proposes the characteristics of "recording the data in one block out of two starting from a first block, following the triggering of the reading of the data, alternately of reading a previously recorded block and of continuing the recording in the block following the block read". That is, the invention of the Applicant is directed at least in part to solving the deficiencies of the invention of Thomason which needs and teaches an additional buffer (35). As such, the Applicant respectfully submits that the invention of the Applicant, at least with respect to claim 1, is a totally different solution than the one proposed in Thomason as Thomason does not teach, suggest or anticipate recording data in one block out of two, wherein the recording is carried out on a medium organized in the form of logic blocks. That is, Thomason absolutely fails to teach, suggest or anticipate "recording data in one block out of two starting from a first block" where the blocks are blocks of a recording medium as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1.

Instead, in Thomason there is a buffer separated in two areas that the Examiner considers as equivalent to the blocks of the recording medium of the

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Applicant's claim 1. However, in Thomason, there is only one block for recording and one block for reading and they are not blocks of the main memory 36 (medium organized in the form of logic blocks) as taught and claimed by the Applicant, but instead are portions of the buffer 35. As such, the Applicant respectfully submits that Thomason absolutely fails to teach, suggest or anticipate the invention of the Applicant, at least with respect to claim 1, where it is clear that the main memory (medium organized in the form of logic blocks) comprises several blocks and that during a write operation, data is written leaving a free space in the data block chain for subsequent recording, the free space being a block as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1.

As such, the Applicant submits that this is clearly a structural difference between the claimed invention and the cited prior art of Thomason. That is, in Thomason, there is clearly a need for an external memory buffer, and in contrast, in the invention of the Applicant, there is no need for such a buffer due to the characteristics of claim 1. More specifically, in Thomason, it is the main memory which comprises a single reading and writing head and the blocks are not blocks of the main memory but blocks of the buffer located between the main memory 36 and the microprocessor. In contrast, in the invention of the Applicant, there is a main memory comprising a single reading and writing head and this main memory is separated into logic blocks. The Applicant's teachings describe the management of this main memory during recording of data using a new inventive method of block management avoiding the loss of time during the switch between read and write operations and without the need of an external buffer as disclosed in Thomason.

Therefore, the Applicant submits that for at least the reasons recited above, independent claim 1 is not anticipated by the teachings of Thomason and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claim 7 recites similar relevant features as recited in the Applicant's independent claim 1. More specifically, claim 7 recites "an interfacing circuit for interfacing the recording medium with said control circuit, said control circuit initially instructing the recording of data in one block out of two starting from a first block and subsequently, following the triggering of the reading

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of the data, alternately the reading of a block previously recorded and the continuing of the recording in the block following a block read". As described above, there is absolutely no teaching, suggestion or disclosure in Thomason for at least "recording data in one block out of two starting from a first block" as claimed by the Applicant's independent claims 1 and 7. As such, the Applicant respectfully submits that for at least the reasons recited above independent claim 7 is also not anticipated by the teachings of Thomason and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 2-4 and 6 depend directly from independent claim 1 and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicant submits that dependent claims 2-4 and 6 are also not anticipated by the teachings of Thomason. Therefore the Applicant submits that dependent claims 2-4 and 6 also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

In addition, the Applicant reiterates his arguments of the previous response. More specifically, in Thomason the blocks are not arranged in logic blocks in buffers. Secondly, Thomason fails to teach, suggest or make obvious that the buffer is arranged by recording one address out of two starting from a first address, as claimed by at least the Applicant's independent claim 1. The Examiner cites col. 4 lines 47-51, col. 5 lines 7-26 and FIG. 3 in Thomason for anticipating the Applicant's claim 1, however, these passages are not relevant as they only disclose that the data is transferred from the buffer to the disk when the disk is capable of receiving the data. Col 5 lines 7-26 of Thomason also only discloses normal buffer management and not buffer management as taught in the Applicant's Specification and claimed by at least the Applicant's independent claim 1. Even further, Thomason fails to teach, suggest or anticipate "following the triggering of the reading of the data, alternately reading a previously recorded block and continuing the recording in the block following the block read" as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. Instead, Thomason merely teaches the reading of data in the main memory and

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this reading is just reading the data when the disk is ready. Thomason further teaches supplying the buffer memory before sending them to a TV screen.

As such and for at least the reasons described above and specifically because Thomason fails to teach, suggest or anticipate at least "recording data in one block out of two starting from a first block" and "following the triggering of the reading of the data, alternately reading a previously recorded block and continuing the recording in the block following the block read" as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1, the Applicant respectfully submits that Thomason fails to teach, suggest or disclose at least each and every element of the Applicant's claimed invention, arranged as in at least the Applicant's claim 1 as required for anticipation. Therefore, the Applicant respectfully submits that the teachings and disclosure of Thomason do not anticipate the Applicant's invention, at least with respect to independent claim 1.

Therefore, the Applicant submits that for at least the reasons recited above, independent claim 1 is not anticipated by the teachings of Thomason and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claim 7 recites similar relevant features as recited in the Applicant's independent claim 1. More specifically, claim 7 recites "an interfacing circuit for interfacing the recording medium with said control circuit, said control circuit initially instructing the recording of data in one block out of two starting from a first block and subsequently, following the triggering of the reading of the data, alternately the reading of a block previously recorded and the continuing of the recording in the block following a block read". As described above, there is absolutely no teaching, suggestion or disclosure in Thomason for at least "recording data in one block out of two starting from a first block" and "following the triggering of the reading of the data, alternately reading a previously recorded block and continuing the recording in the block following the block read" as claimed by the Applicant's independent claims 1 and 7. As such, the Applicant respectfully submits that for at least the reasons recited above independent claim 7 is also not anticipated by the teachings of Thomason and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

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Furthermore, dependent claims 2-4 and 6 depend directly from independent claim 1 and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicant submits that dependent claims 2-4 and 6 are also not anticipated by the teachings of Thomason. Therefore the Applicant submits that dependent claims 2-4 and 6 also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

B. 35 U.S.C. § 103

The Examiner rejected claims 5 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Thomason in view of Mishara (U.S. Patent No. 6,304,927). The rejection is respectfully traversed.

The Examiner applied Thomason for the rejection of claims 5 and 8 as applied above for the rejection of claims 1-4, 6 and 7. As described above, Thomason absolutely fails to teach, suggest or anticipate at least the Applicant's independent claims 1 and 7. As such, and at least because Thomason fails to teach, suggest or anticipate the Applicant's independent claims 1 and 7, the Applicant further submits that Thomason also fails to teach, suggest or anticipate the Applicant's claims 5 and 8, which depend directly from the Applicant's claims 1 and 7, respectively.

Furthermore, the Applicant submits that Mishara also fails to teach, suggest or render obvious at least "recording data in one block out of two starting from a first block" and "following the triggering of the reading of the data, alternately reading a previously recorded block and continuing the recording in the block following the block read" as taught in the Applicant's Specification and claimed by at least the Applicant's independent claims 1 and 7. That is, the teachings of Mishara for a digital copier or multi-function device with a scalable architecture fails to teach, suggest or render obvious at least "recording data in one block out of two starting from a first block" and "following the triggering of the reading of the data, alternately reading a previously recorded block and continuing the recording in the

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block following the block read" as taught in the Applicant's Specification and claimed by at least the Applicant's independent claims 1 and 7.

As such, the Applicant submits that at least because Mishara fails to teach, suggest or render obvious at least the Applicant's independent claims 1 and 7, the Applicant further respectfully submits that Mishara also fails to teach, suggest or render obvious the Applicant's claims 5 and 8, which depend directly from the Applicant's independent claims 1 and 7, respectively.

Furthermore, the Applicant submits that there is absolutely no motivation or suggestion in either reference for the combination of Thomason and Mashira to attempt to teach the invention of the Applicant. More specifically, there is no motivation or suggestion in the invention of Mashira for the combination of the references and likewise, the invention of Thomason does not expressly or impliedly motivate or suggest such a combination as required by for the combination of references under 35 U.S.C. § 103.

Even further, the Applicant submits that even if there was a motivation to combine the references (which the Applicant maintains that no such motivation exists), the teachings of Mashira fail to bridge the substantial gap between the teachings of Thomason and the Applicant's invention at least with respect to independent claims 1 and 7.

As such and for at least the reasons recited above, the Applicant respectfully submits that the teachings of Thomason and Mashira, alone or in any allowable combination, fail to teach, suggest or make obvious the invention of the Applicant with regard to at least the Applicant's independent claims 1 and 7. As such, the Applicant further submits that the teachings of Thomason and Mashira, alone or in any allowable combination, also fail to teach, suggest or make obvious the invention of the Applicant with regard to dependent claims 5 and 8, which depend directly from the Applicant's independent claims 1 and 7, respectively, and recite further limitations thereof.

Therefore, the Applicant submits that for at least the reasons recited above, the Applicant's claims 5 and 8 are not rendered obvious by the teachings of Thomason and Mishara, alone or in any allowable combination and, as such, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

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Conclusion

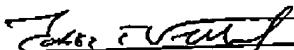
The Applicant respectfully submits that none of the claims, presently in the application, are anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. § 103. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, or if the Examiner believes a telephone interview would expedite the prosecution of the subject application to completion, it is respectfully requested that the Examiner telephone the undersigned.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account No. 07-0832.

Respectfully submitted,
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